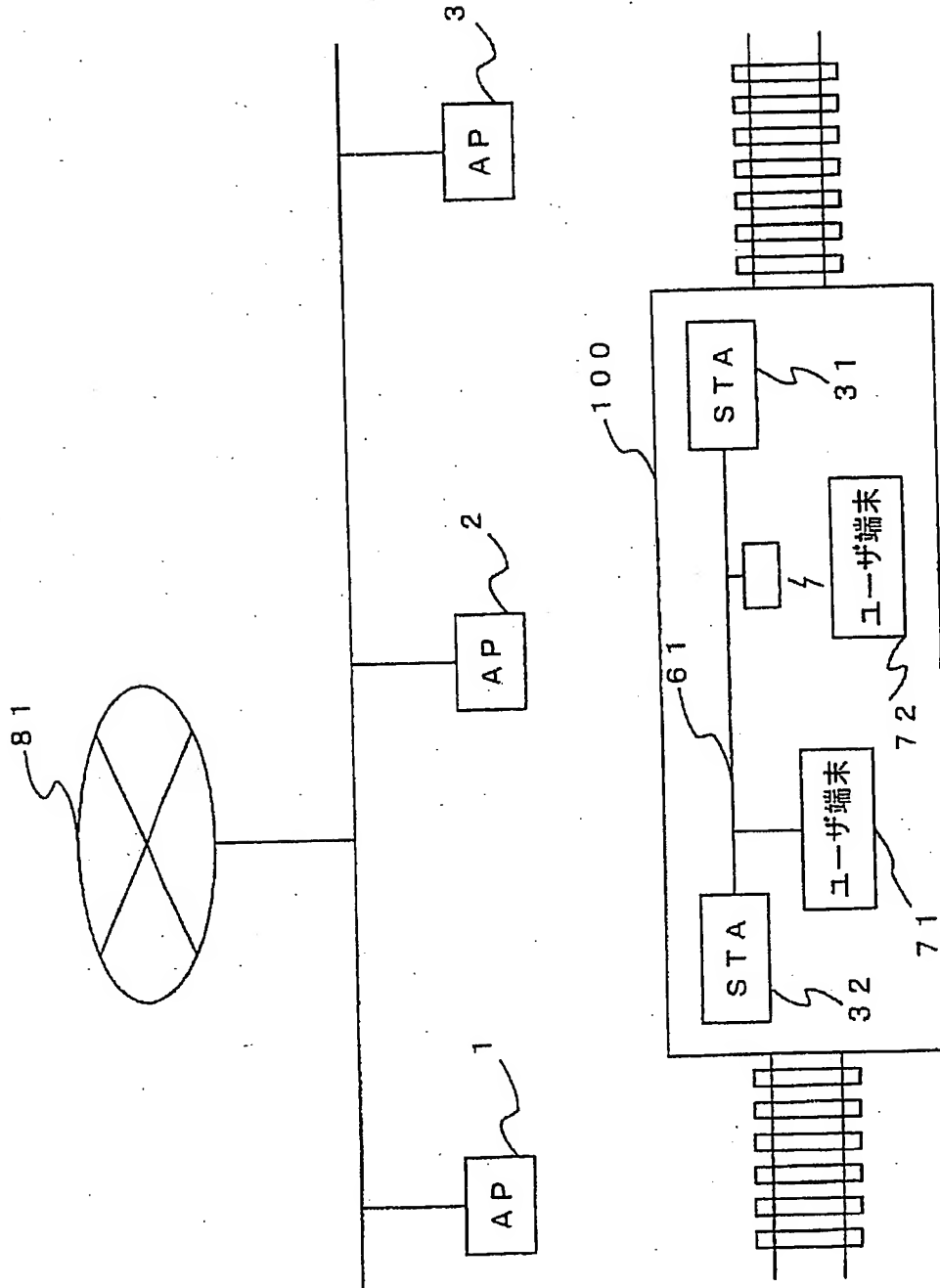


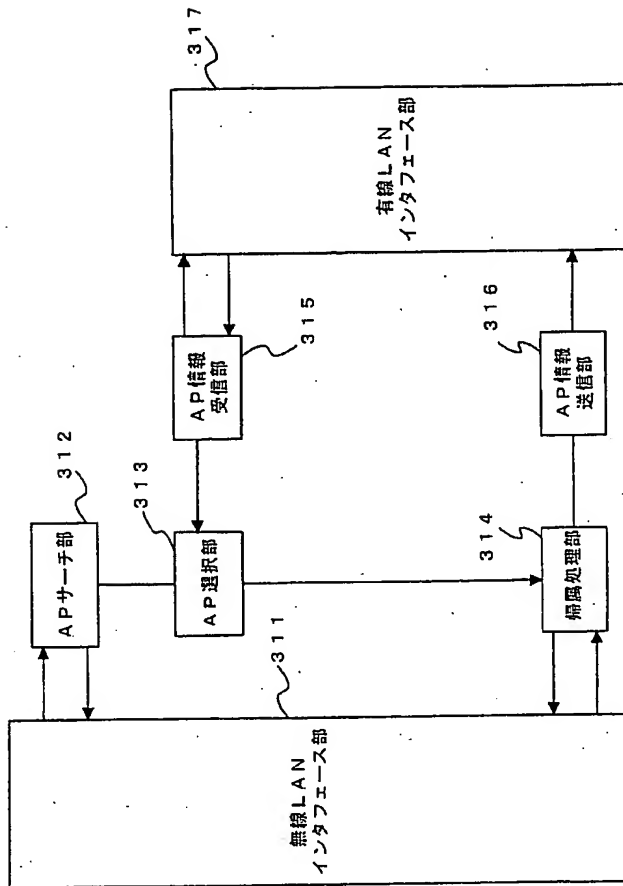
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[図1]

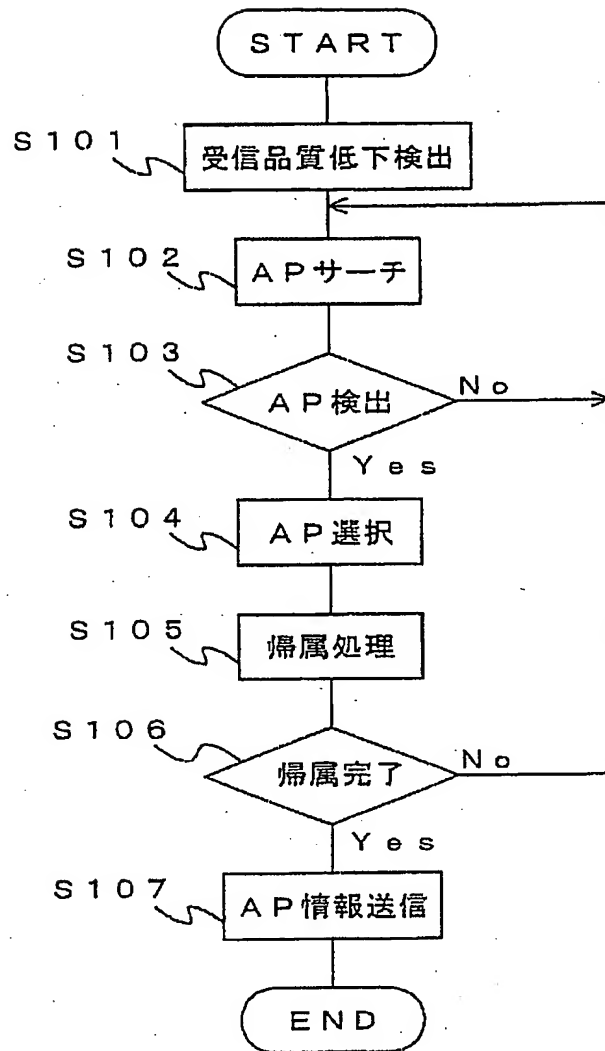


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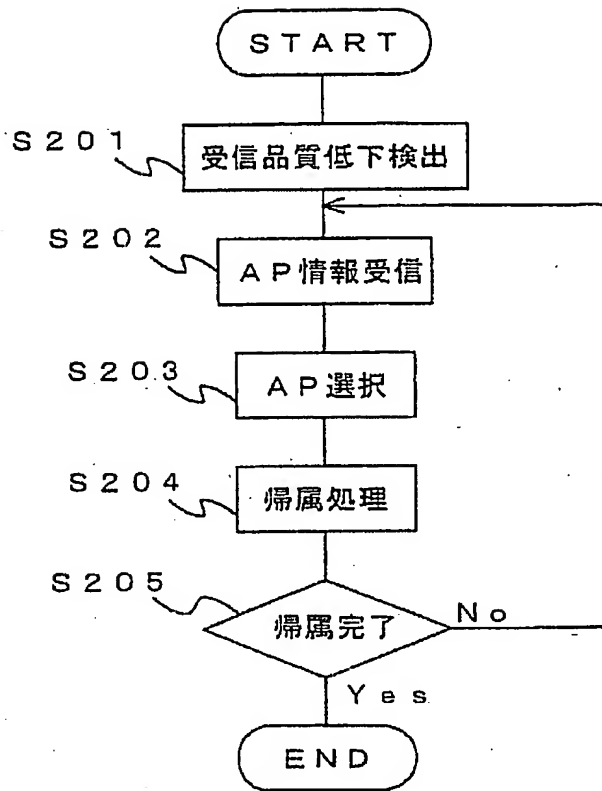
[図2]



[図3]

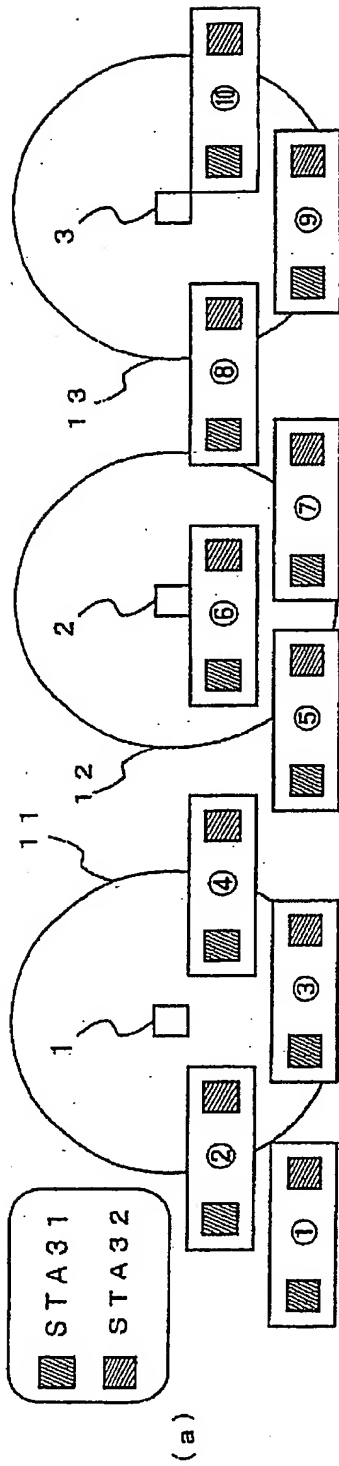


[図4]



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[図5]



(c)

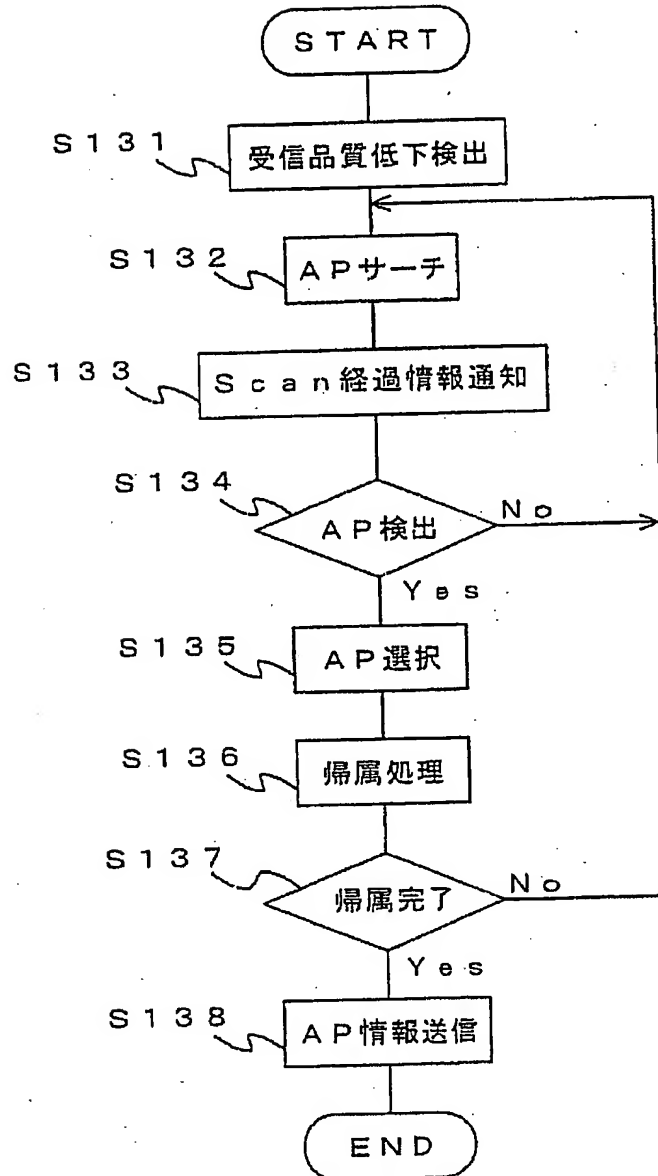
本発明	3 1	31→32	3 2
①	Scan	-	Scan
②	Scan→AP1	-	Scan
③	AP1	-	Scan→AP1
④	Scan	-	AP1
⑤	Scan→AP2	-	Scan
⑥	AP2	-	Scan→AP2
⑦	Scan	-	AP2
⑧	Scan→AP3	-	Scan
⑨	AP3	-	Scan→AP3
⑩	Scan	-	AP3

(b)

本発明	3 1	31→32	3 2
①	Scan	-	-
②	Scan→AP1	AP1	-
③	AP1	-	AP1
④	Scan	-	AP1
⑤	Scan→AP2	AP2	-
⑥	AP2	-	AP2
⑦	Scan	-	AP2
⑧	Scan→AP3	AP3	-
⑨	AP3	-	AP3
⑩	Scan	-	AP3

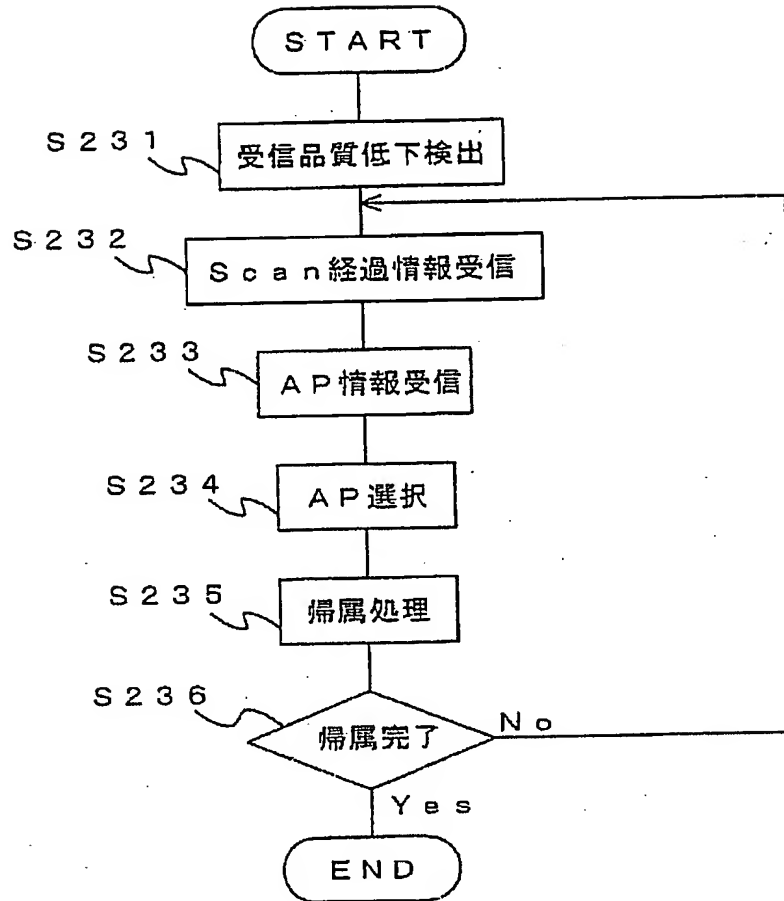
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[図6]



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[図7]

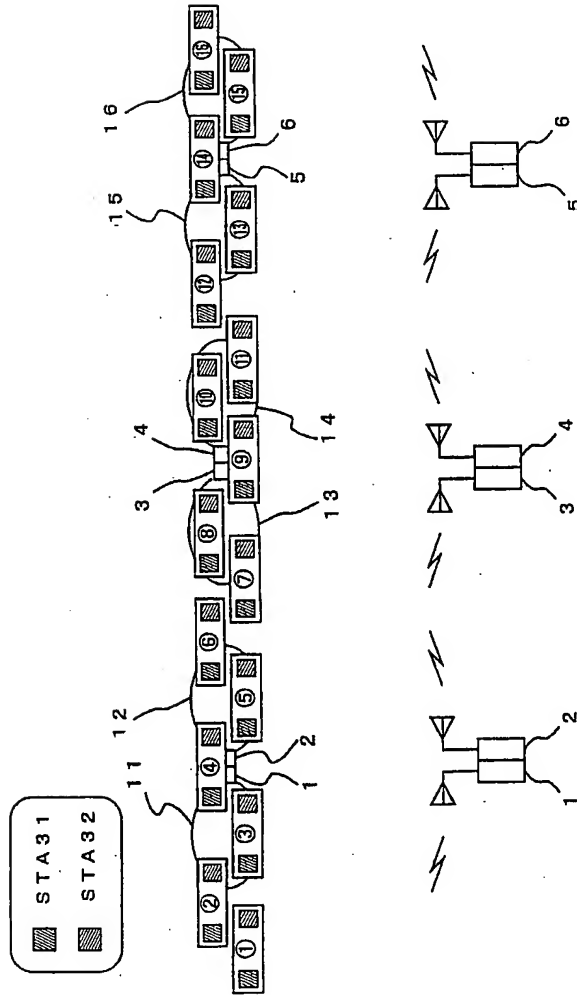


本発明	31	31→32	32
①	Scan all	f1~fa: x	Scan fa+1~f14
②	Scan all→AP1	f1~f5: x	Scan f6~f14→AP1
③			
④	Scan all	f1~fb: x	AP1
⑤	Scan all→AP2	f1~f8: x	Scan f9~f14→AP2
⑥			
⑦	Scan all		AP2
⑧	Scan all→AP3	AP3	AP3
⑨			
⑩	Scan all	f1~fc: x	AP3

Figure 1 shows the block diagrams for STA 31 and STA 32. STA 31 is a 14-bit parallel adder with inputs f1 through f14 and a carry-in. STA 32 is a 14-bit parallel adder with inputs f1 through f14 and a carry-in from STA 31. The carry-in to STA 32 is the carry-out of STA 31, which is the sum of f14 and the carry-in to STA 31.

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[図10]



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[図11]

本発明	3 1	31→32	3 2
①	Scan	—	—
②	Scan→AP1	AP1	—
③	AP1	—	AP1
④	Scan→AP2	AP2	AP1
⑤	AP2	—	AP2
⑥	Scan	—	AP2
⑦	Scan→AP3	AP3	—
⑧	AP3	—	AP3
⑨	Scan→AP4	AP4	AP3
⑩	AP4	—	AP4
⑪	Scan	—	AP4
⑫	Scan→AP5	AP5	—
⑬	AP5	—	AP5
⑭	Scan→AP6	AP6	AP5
⑮	AP6	—	AP6
⑯	Scan	—	AP6

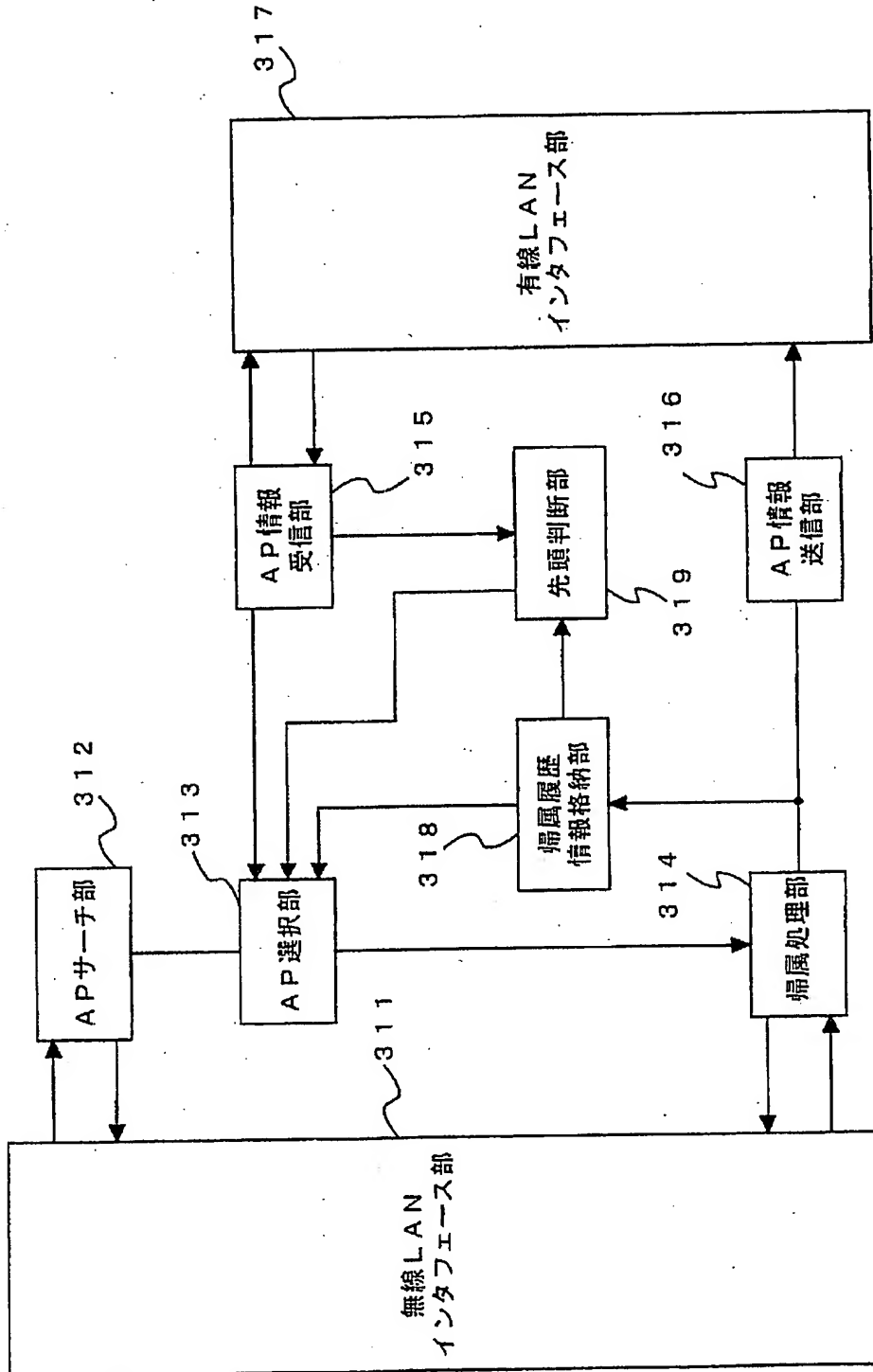
(a)

従来	3 1	31→32	3 2
①	Scan	—	Scan
②	Scan→AP1	—	Scan
③	AP1	—	Scan→AP1
④	Scan→AP2	—	AP1
⑤	AP2	—	Scan→AP2
⑥	Scan	—	AP2
⑦	Scan→AP3	—	Scan
⑧	AP3	—	Scan→AP3
⑨	Scan→AP4	—	AP3
⑩	AP4	—	Scan→AP4
⑪	Scan	—	AP4
⑫	Scan→AP5	—	Scan
⑬	AP5	—	Scan→AP5
⑭	Scan→AP6	—	AP5
⑮	AP6	—	Scan→AP6
⑯	Scan	—	AP6

(b)

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[図12]



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[図13]

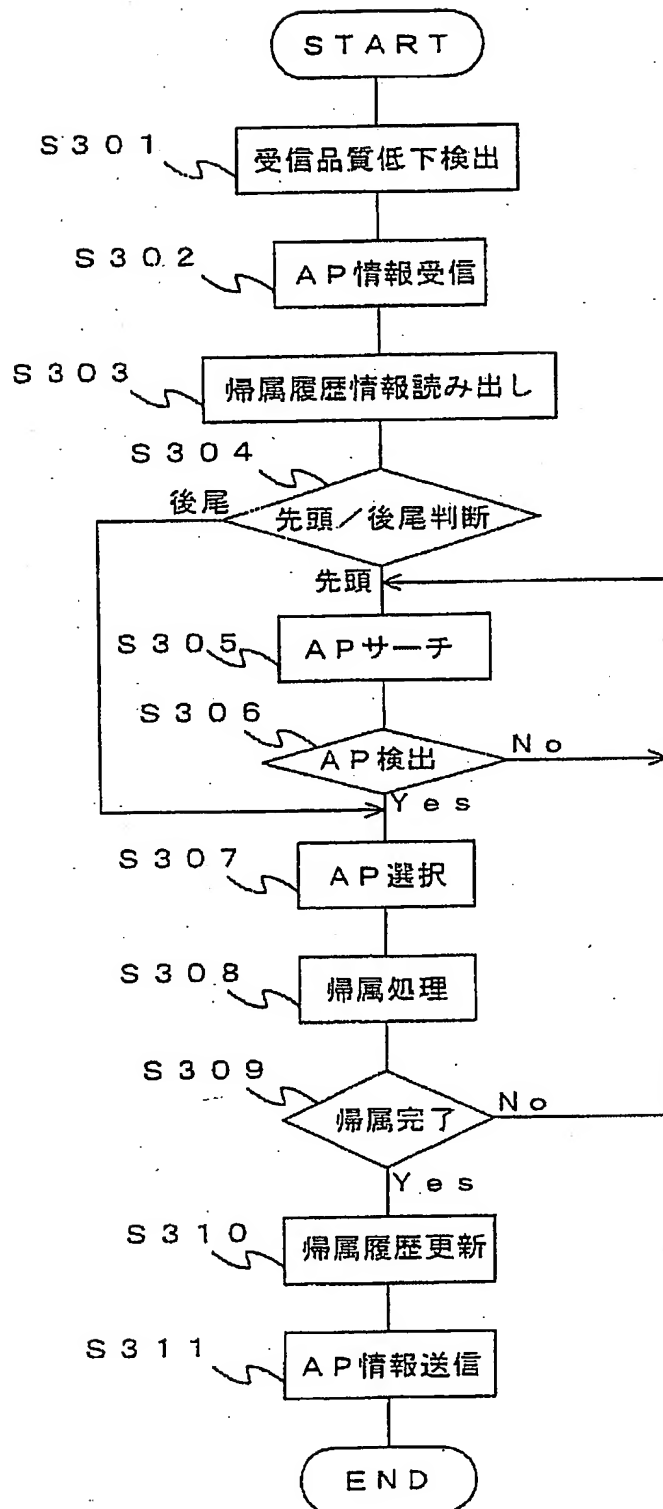
No.	AP識別子	周波数
1	AP5	f1
2	AP4	f14
3	AP3	f11
4	AP2	f6
5	AP1	f1

(a) 帰属履歴情報

No.	AP識別子	周波数
1	AP6	f6
2	AP5	f1
3	AP4	f14
4	AP3	f11
5	AP2	f6
6	AP1	f1

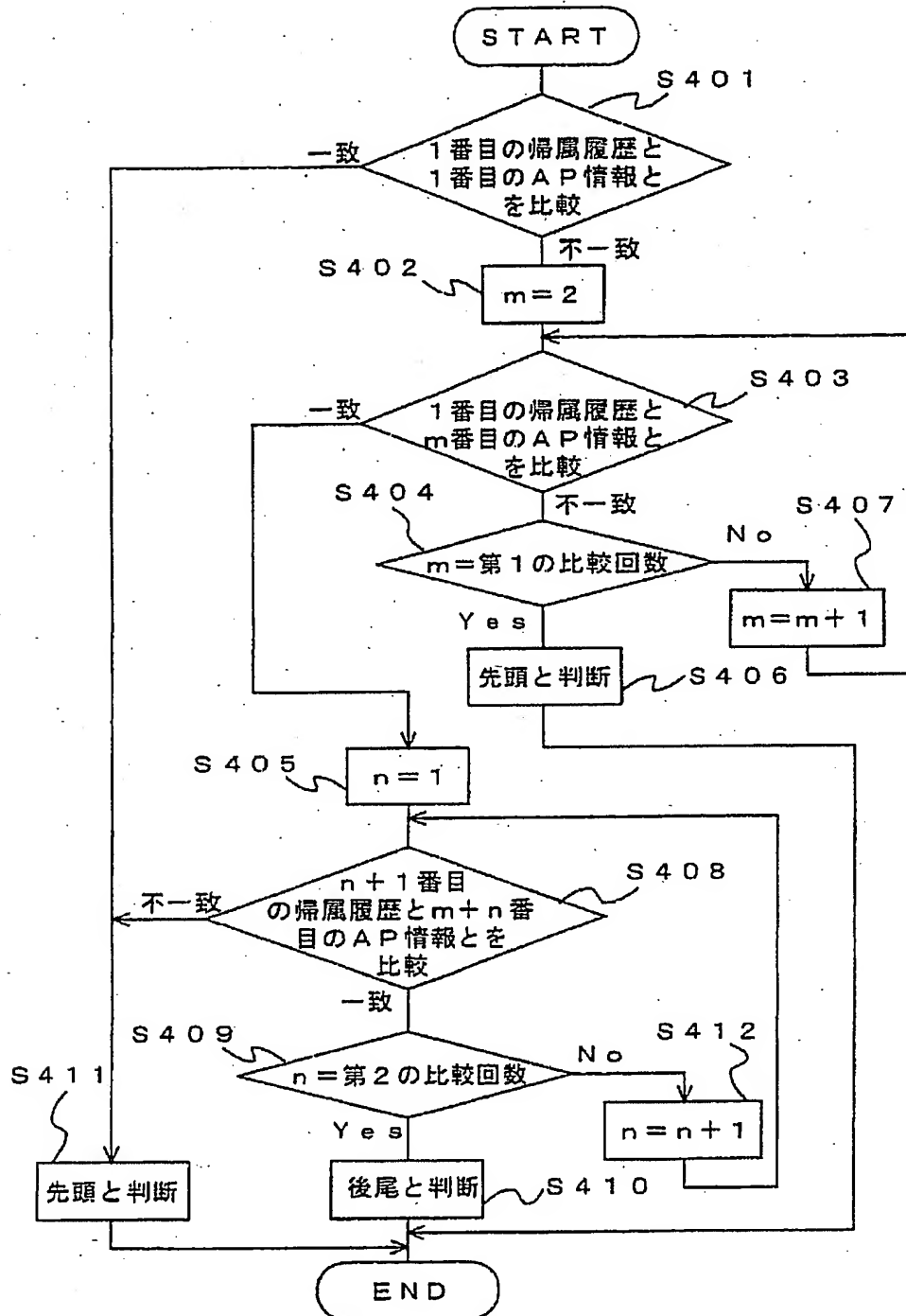
(b) AP情報

[図14]



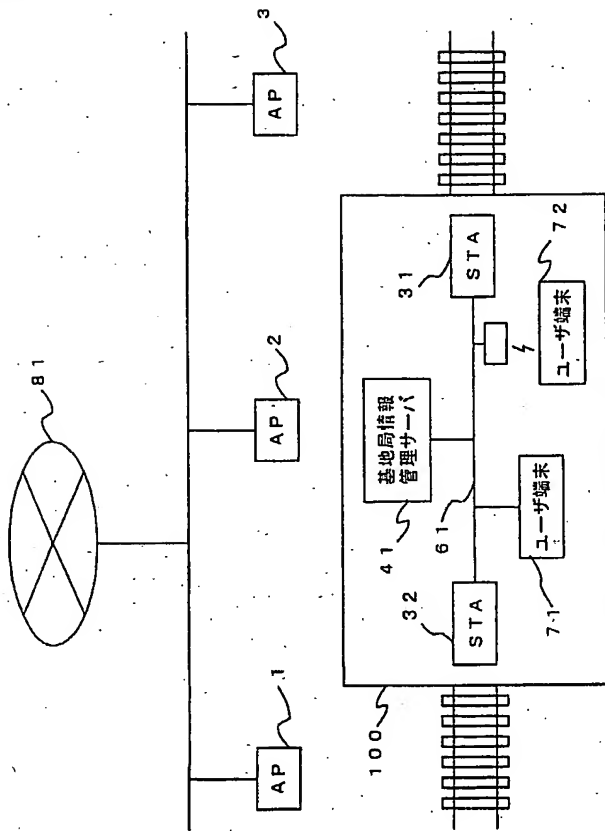
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[図15]



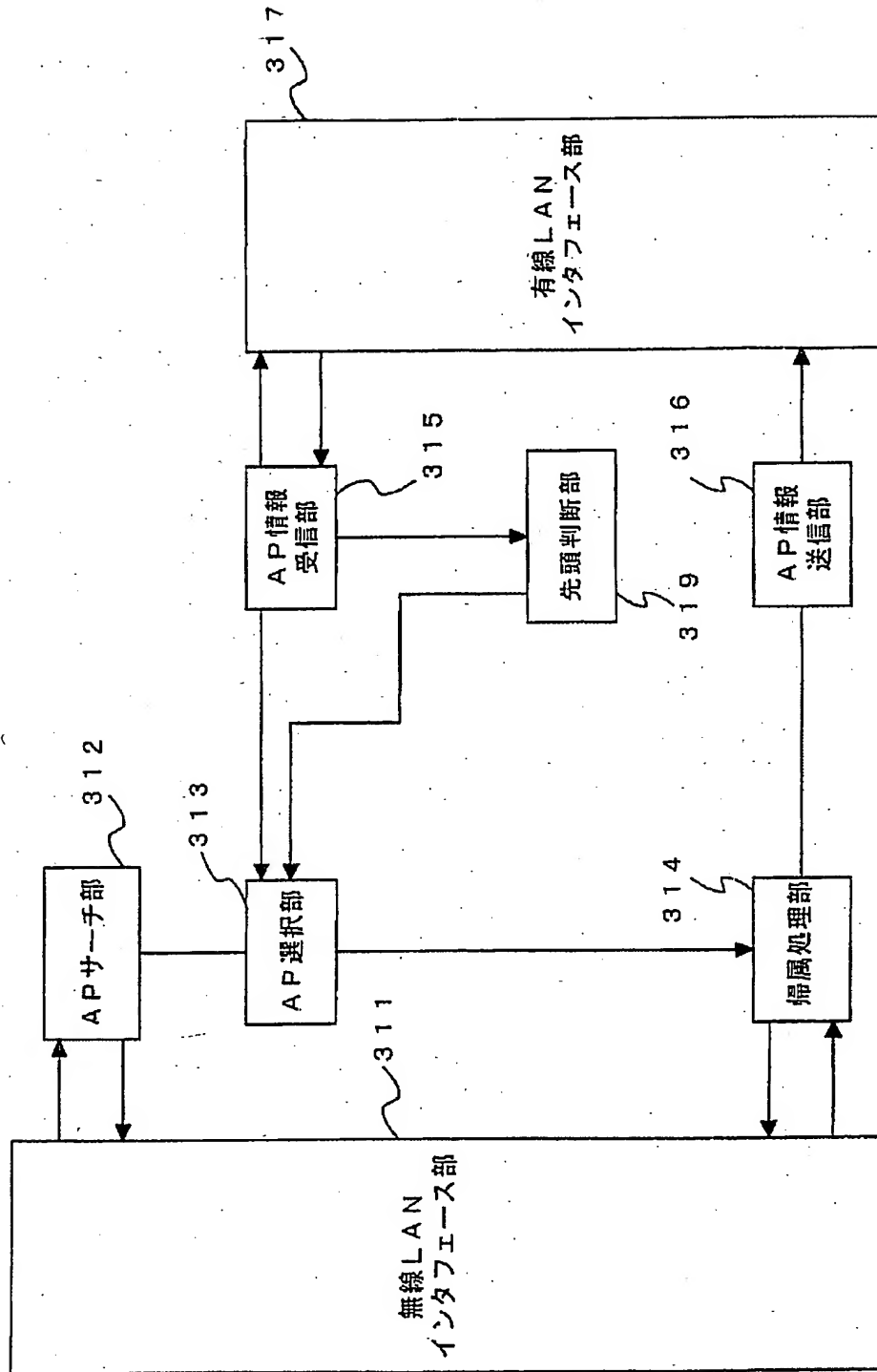
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[図16]



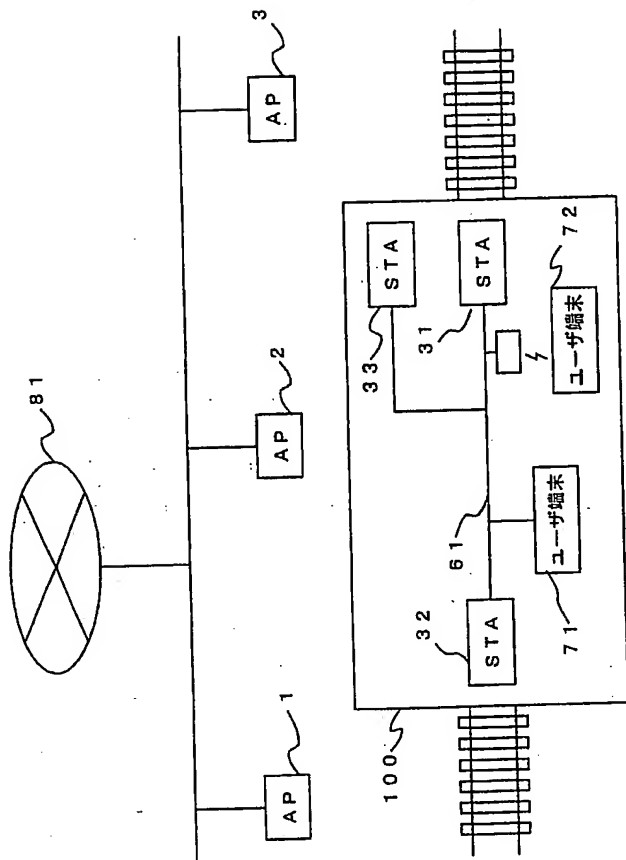
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[図17]



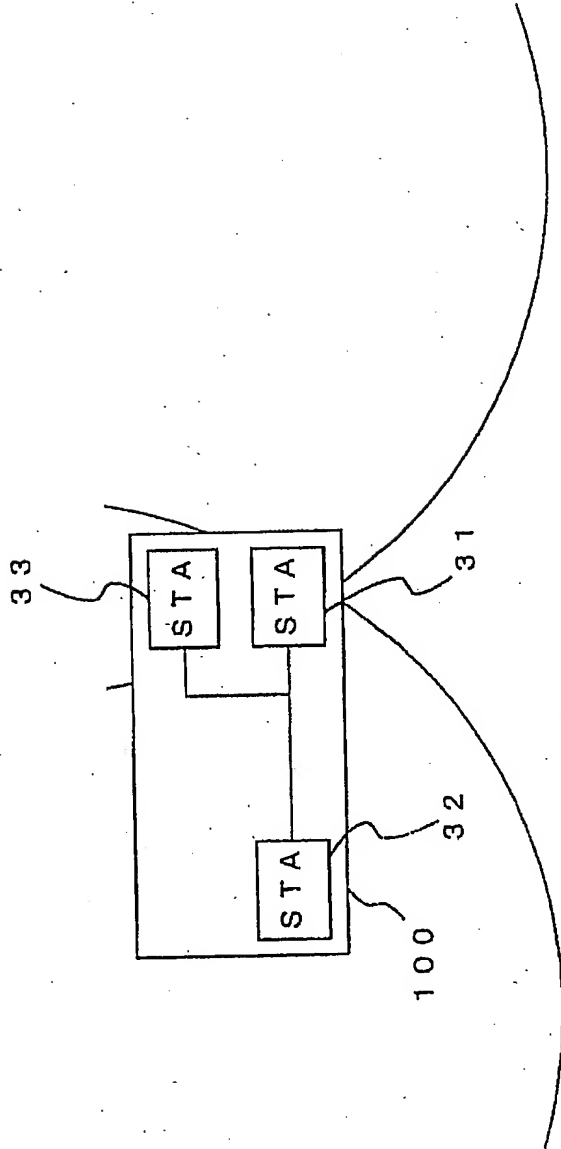
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[図18]



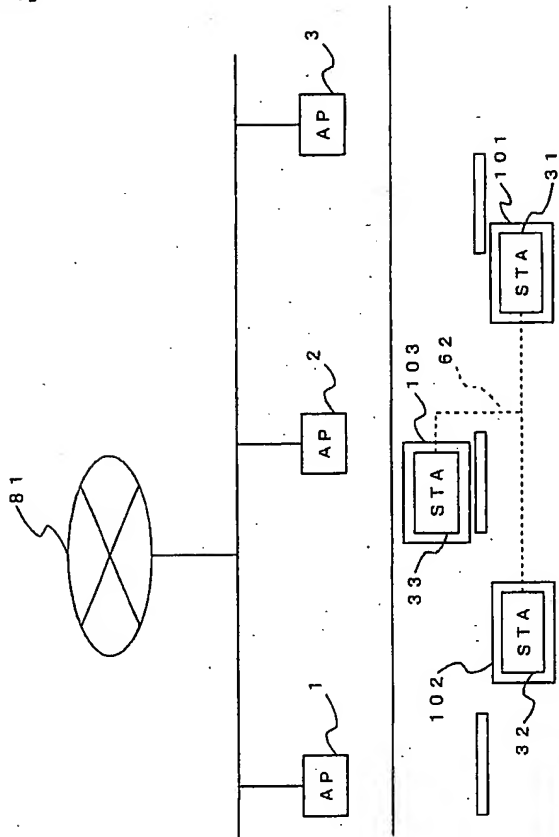
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[19]



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[図20]



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[図21]

